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EXAMINER	
CHAUHAN, ULKA J	
ART UNIT	**PAPER NUMBER**
2676	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/086,174	LAVELLE ET AL.	
	Examiner	Art Unit	
	Ulka J. Chauhan	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) *11-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 33-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 11-32 are withdrawn and claims 41-43 are newly added; claims 1-43 are pending.

Election/Restrictions

2. Claims 11-32 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected inventions, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 6/10/04. The reply filed on 6/10/04 in response to the Office Action requiring election/restriction includes no arguments traversing the restriction; therefore, the election of claims 1-10 is being treated as an election without traverse.

3. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-4, 6, 8-10, 33, 34, 36-39, and 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,579,473 to Schlapp et al and U.S. Patent Application Publication No. 2003/0093744 to Leung et al.

7. As per claim 1, Schlapp discloses a graphics system comprising:

one or more memories configured to receive and store graphics data, wherein each memory comprises on a single integrated chip (Fig. 1: *FBRAM chips 71-82*), one or more RAM memories configured to store the graphics data (Fig. 2: *DRAM banks A-D*), a level two cache memory connected to each RAM memory (Fig. 2: *Page Buffers A-D*; c. 5 ll. 50: *The page buffers A-D comprise the L2 pixel cache*), and a level one cache memory connected to each of the level two cache memories (Fig. 2: *Pixel Buffer 56*; c. 4 ll. 59-61: *The pixel buffer 56 is a high speed, 3 port SRAM and functions as a level one (L1) pixel cache for the FBRAM chip*);

an array of registers configured to store status information, wherein the status information tracks and indicates accesses to the graphics data in the level one cache, wherein the status information further indicates whether the graphics data is modified or unmodified (c. 15 ll. 22-25: *Each entry in the L1 cache table includes a valid bit, a dirty bit, a write only bit, a stateful bit a bank field, a page field, and a column field*; c. 17 ll. 30-31: *The L1 cache tags and the L2 cache tags indicate the state of the L1 and L2 pixel caches in the FBRAM chips*; c. 18 ll. 14-17: *The L1 cache tags provide information similar to the L1 cache table but with more current state information for the FBRAM chips*); and

a memory request processor connected to the memories and to the array of registers, wherein the memory request processor is operable to write-back graphics data stored in one of the

level one cache memories that the status information indicates is modified to one of the corresponding level two cache memories (c. 12 ll. 14-20: *The frame buffer memory device controller 83 ensures that modified blocks in the L1 pixel cache are appropriately written back into the L2 pixel cache*).

8. As per claim 1, Schlapp does not expressly teach that the graphics data are written-back when an empty memory cycle occurs. This is what Leung teaches. Leung discloses that the write-back operations are performed during idle cycles when no external memory access is requested, such that the write back operation does not impose a penalty on memory cycle time or affect memory access latency (Abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Leung and Schlapp such that the modified blocks in Schlapp's L1 pixel cache are appropriately written back into the L2 pixel cache during idle cycles, as taught by Leung, so that the write back operation does not impose a penalty of memory cycle time and affect the memory access latency.

9. As per claims 2 and 3, Schlapp discloses that the graphics data comprises samples and pixels (c. 3 ll. 60-62: *The rendering processor 70 writes pixel data to the FBRAM chips through the frame buffer memory device controller 83; since the pixel data includes a value for that pixel, the value in considered the sample for that pixel*).

10. As per claim 4, Schlapp discloses that each level one cache memory is divided into logical blocks, and wherein each register of status information corresponds to one logical block (c. 4 ll. 65: *The L1 pixel cache comprises a set of L1 cache blocks*; c. 5 ll. 36-38: *The eight L1 cache blocks also correspond to eight set of dirty tag bits in the dirty tags memory*; c. 15 ll. 22-27: *Each entry in the L1 cache table includes a valid bit (V), a dirty bit (D), a write only bit (W),*

a stateful bit (S), a bank field, a page field, and a column field. The dirty bit indicates that the corresponding block of the L1 pixel cache contains updated pixels which must be written back to the L2 pixel cache before the L1 block can be reallocated).

11. As per claim 6, Schlapp discloses a request queue connected to the memory request processor, wherein the request queue comprises a first-in-first-out (FIFO) storage structure, wherein the request queue is configured to receive and buffer memory requests, and wherein the request queue is further configured to output the memory requests to the memory request processor in response to control signals from the memory request processor (c. 13 ll. 30-34: *Scheduler circuit 320 within the frame buffer memory device controller 83, buffers the L1 cache request, and the L2 cache request in separate internal first-in-first-out (FIFO) memory queues. The separate memory queues operate independently*; c. 13 ll. 64-66: *The arbiter circuit 330 within the frame buffer memory device controller 83, issues L1 cache requests, L2 cache requests, and video transfer operation requests to the FBRAM chips 71-82 over the DRAM operation bus 110. The arbiter circuit 330 arbitrates the L1 cache requests, and the L2 cache requests from the scheduler circuit 320*).

12. As per claim 8, Schlapp discloses a shift register connected to each RAM, wherein each shift register is configured to receive and store portions of the graphics data from each RAM, and wherein each shift register is further configured to output graphics data serially in response to an external clock signal (c. 4 ll. 54-58: *The video buffer 52 receives data from the page buffers A and C. The video buffer 54 receives data from the page buffers B and D. The data in the video buffers 52 and 54 is shifted out over the video bus 134 to the video output circuit 84 through a multiplexer 62*; c. 8 ll. 24-26 and Fig. 2: *The video data transferred over the video bus 134 is*

synchronized by the VID_ CLK signal. The VID_ CLK signal is a gated or free-running video shift clock).

13. As per claim 9, Schlapp discloses a display device, wherein the display device displays images according to the graphics data (c. 3 ll. 32-34: *Each FBRAM chip 71-82 also contains a pair of video buffers that perform CRT refresh operations for a display device*).

14. As per claim 10, Schlapp discloses that each memory further comprises an arithmetic logic unit (ALU) connected to the level one cache memory (Fig. 2: *pixel ALU 58 connected to pixel buffer 56*), wherein the ALU is configured to: receive as one operand graphics data from a source external to the memory; receive as a second operand graphics data stored in the level one cache; arithmetically combine the two operands according to a function defined by an external control signal; and store the results of the arithmetic combination in the level one cache (c. 3 ll. 36-45: *The pixel ALU in each FBRAM chip 71-82 includes a set of four raster operations units. Each raster operation unit performs selectable raster operations on each individual byte of pixel data transferred to the corresponding SRAM pixel buffer. The pixel ALU in each FBRAM chip 71-82 contains a set of four pixel blending units. Each pixel blending unit combines one byte of old internal pixel values with one byte of new pixel values and related information received from the rendering processor 70 according to a series of pipeline processing stages for the pixel ALU*).

15. As per claim 33, Schlapp discloses a global data bus connecting the level one cache memory to each of the level two cache memories (c. 5 ll. 45-48 and Fig. 2: *parallel transfer of an entire L1 cache block between the page buffers A-D and the pixel buffer 56 over global bus 60*).

Remaining elements of claims 33, 36, 37, and 38 are similar in scope to claims 1-4 and are rejected under the same rationale.

16. As per claim 34, Schlapp discloses that the transfer of graphics data is prompted on demand (c. 15 ll. 63-66: *If the entry in the L1 cache table specified by the least recently allocated counter 400 is dirty, then the allocator circuit 310 issues an L1 cache request to the scheduler circuit 320 to write back the dirty block*).

17. As per claim 39, Schlapp discloses the memory request processor is further operable to transfer graphics data from any level one cache memory to a corresponding level two cache memory and at the same time to the RAM memory connected to the level two cache memory (c. 12 ll. 14-20: *The frame buffer memory device controller 83 ensures that modified blocks in the L1 pixel cache are appropriately written back into the L2 pixel cache over the global busses of the FBRAM chips 71-82. The frame buffer memory device controller 83 also ensures that pages in the L2 pixel cache are returned to the DRAM cores of the FBRAM chips 71-82 as appropriate*).

18. As per claim 41, Schlapp teaches a method for write-back of modified graphics data, the method comprising:

a) testing a dirty tag bit corresponding to a block of graphics data currently under examination in a level one cache, wherein the dirty tag bit indicates whether the data in the block is modified; b) reading a dirty tag bit corresponding to a next block of graphics data in the level one cache, if the dirty tag bit indicates that the current block is not modified (c. 15 ll. 23-28: *Each entry in the L1 cache table includes a dirty bit (D)... The dirty bit indicates that the corresponding block of the L1 pixel cache contains updated pixels*

which must be written back to the L2 pixel cache before the L1 block can be reallocated; c. 16 ll. 22-24: *the allocator circuit 310 checks the dirty bit of the specified entry in the L1 cache table to determine whether a write back operation is required*);

d) commanding a memory request processor to write-back the current block of graphics data from the level one cache to a corresponding level two cache (c. 15 ll. 63-66: *the allocator circuit 310 issues an L1 cache request to the scheduler circuit 320 to write back the dirty block*);

e) modifying the dirty tag bit corresponding to the current block of graphics data to indicate that the block is no longer modified and is available for future allocation (c 15 ll. 52-53 and c. 16 ll. 2-3: *the specified entry of the L1 cache table is set to clean*); and

f) repeating steps a) through e) for the next block of graphics data in the level one cache (c. 15 ll. 38-44: *the allocator circuit compares the incoming bank page and column parameters from the translator circuit to all six entries in the L1 cache table simultaneously... if the incoming do not correspond to an entry, the least recently allocated entry is written back to the L2 cache if it is indicated to be dirty*).

19. As per claim 41, Schlapp does not expressly teach c) stalling until an empty memory cycle is detected, if the dirty tag bit indicates that the current block is modified, or write-back when the empty memory cycle occurs. This is what Leung teaches. Leung discloses that write-back operations are performed during idle cycles when no external memory access is requested, such that the write back operation does not impose a penalty on memory cycle time or affect memory access latency (Abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Leung and Schlapp such

that the write-back of modified blocks in Schlapp's invention is stalled until an idle cycle occurs, and modified L1 pixel cache blocks are appropriately written back into the L2 pixel cache during idle cycles, as taught by Leung, so that the write back operation does not impose a penalty of memory cycle time and affect the memory access latency.

20. As per claim 42, Schlapp discloses that the level two cache is configured as a "write-through" cache, and as the current block is written to the level two cache it is also written through to an associated DRAM memory bank connected to the level two cache (c. 5 ll. 55-59: *The L2 pixel cache employs a write through policy. Pixel data written into a L2 pixel cache entry over the global bus 60 is transferred immediately into the corresponding page of the corresponding DRAM bank A-D*).

21. As per claim 43, Schlapp does not expressly teach that the transfer of graphics data occurs each time there is modified graphics data in the level one cache, and there is an empty cycle on the global data bus. Leung discloses that write-back operations are performed during idle cycles when no external memory access is requested, such that the write back operation does not impose a penalty on memory cycle time or affect memory access latency (Abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Leung and Schlapp such that the write-back of modified blocks in Schlapp's invention occurs only during idle cycles, as taught by Leung, so that the write back operation does not impose a penalty of memory cycle time and affect the memory access latency.

22. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,579,473 to Schlapp et al, U.S. Patent Application Publication No. 2003/0093744 to Leung et al, and U.S. Patent No. 6,415,358 to Arimilli et al.

23. As per claim 5, Schlapp discloses:

a dirty block bit, wherein the dirty block bit indicates which portions of the graphics data in the level one cache memory has been modified (c. 15 ll. 22-27: *Each entry in the L1 cache table includes a valid bit (V), a dirty bit (D), a write only bit (W), a stateful bit (S), a bank field, a page field, and a column field. The dirty bit indicates that the corresponding block of the L1 pixel cache contains updated pixels which must be written back to the L2 pixel cache before the L1 block can be reallocated*).

Schlapp does not expressly teach:

a least recently used (LRU) count, wherein the LRU count indicates which logical block in each level one cache memory has been least recently accessed.

Armilli discloses that cache lines stored within data array 34 are recorded in cache directory 32, which contains one directory entry for each way in data array 34. Each directory entry comprises a tag field 40, coherency status field 42, least recently used (LRU) field 44, and inclusion field 46. LRU field 44 indicates how recently the corresponding way of data array 34 has been accessed relative to the other ways of its congruence class, thereby indicating which cache line should be cast out of the congruence class in response to a cache miss.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Schlapp, Leung, and Armilli whereby an LRU field is included in the L1 cache table entry, so that the corresponding L1 cache block can be easily identified based on how recently it has been accessed for replacement.

24. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,579,473 to Schlapp et al, U.S. Patent Application Publication No. 2003/0093744 to Leung et al, and U.S. Patent No. 6,437,789 to Tidwell et al.

25. As per claim 7 Schlapp discloses one set of registers stores status information indicative of a current state of the level one cache (c. 15 ll. 22-25: *Each entry in the L1 cache table includes a valid bit, a dirty bit, a write only bit, a stateful bit a bank field, a page field, and a column field*; c. 17 ll. 30-31: *The L1 cache tags and the L2 cache tags indicate the state of the L1 and L2 pixel caches in the FBRAM chips*; c. 18 ll. 14-17: *The L1 cache tags provide information similar to the L1 cache table but with more current state information for the FBRAM chips*). Schlapp does not expressly teach the second set of registers stores status information indicative of the current state of the level one cache plus the predicted results of one or more memory requests pending in the request queue. Tidwell discloses a cache 10 having slots 12 with associated flags including "pending" flag and the "dirty" flag (c. 7 ll. 41-45). If an access to a particular slot 12 of SRAM is in the SRAM FIFO pipeline 316 (FIG. 3), but not yet completed, a "pending" flag 30 is set for that slot (c. 7 ll. 47-49). If there is an address match on any of the pending slots of the write cache, a hit condition exists, and no DRAM access is required and the data will be read from the slot (c. 8 ll. 29-31). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Schlapp, Leung, and Tidwell whereby a second set of entries for the L1 cache table is provided to include a pending flag as taught by Tidwell in order to indicate a pending request and to obviate additional DRAM accesses when the requested address matches a pending slot thereby conserving memory accesses.

26. Claims 35 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,579,473 to Schlapp et al, U.S. Patent Application Publication No. 2003/0093744 to Leung et al, and U.S. Patent No. 5,787,473 to Vishlitzky et al.

27. As per claim 35, Schlapp discloses that if the entry in the L1 cache table specified by the least recently allocated counter 400 is dirty, then the allocator circuit 310 issues an L1 cache request to the scheduler circuit 320 to write back the dirty block (c. 15 ll. 63-66). Schlapp does not expressly teach that the transfer of graphics data is periodic. Vishlitzky discloses a cache management system in which a cache manager program performs stage tasks (priority tasks) and de-stage tasks (background tasks) where it is desirable to elevate the de-stage task to a priority task for servicing pending writes when a large number of such pending write requests exist. For example, the device controller executes a high-priority timer-driven interrupt procedure for periodically checking the number of write-back requests in each of the pending write data structures that it services, and for servicing each pending write data structure found to have a number of write-back requests exceeding a certain threshold. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Schlapp and Vishlitzky whereby dirty blocks in the L1 cache are periodically written back so that update data is available in the L2 cache and the DRAM banks and so that additional blocks are available in the L1 cache for replacement.

28. Claim 40 is similar in scope to claim 35 and is rejected under the same rationale.

Response to Arguments

29. Applicant's arguments filed 5/5/05 have been fully considered but they are not persuasive. With respect to the independent claims 1, 33,40, and 41, Applicant argues that the

cited prior art fails to teach writing back data from the L1 cache to the L2 cache when an empty memory cycle occurs. As detailed above, Leung discloses writing back data during idle cycles when no external memory access is requested, and provides the motivation for modifying Schlapp for performing write-back operations during idle cycles for the advantage of not imposing a penalty on memory cycle time or affecting memory access latency (Abstract).

Conclusion

30. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ulka J. Chauhan whose telephone number is 571-272-7782. The examiner can normally be reached on Mon. through Fri., 9:30 a.m. to 4:00 p.m.

32. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 571-272-7778. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

33. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ulka J. Chauhan
Primary Examiner
Art Unit 2676

ujc
May 18, 2005